Notice of Allowability	Application No.	Applicant(s)	
	10/821,848	MIYATA ET AL.	
	Examiner	Art Unit	
	CON P. TRAN	2614	
The MAILING DATE of this communication appeal All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIOF of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in or other appropriate commitmed GHTS. This application is and MPEP 1308.	n this application. If not included unication will be mailed in due cours	
<ol> <li>The allowed claim(s) is/are 8,12-14,22,26-29,33-35,43-46,</li> </ol>	_	27.00	
3. Acknowledgment is made of a claim for foreign priority unal All b) ☐ Some* c) ☐ None of the:  1. Certified copies of the priority documents have 2. ☐ Certified copies of the priority documents have 3. ☐ Copies of the certified copies of the priority documents have International Bureau (PCT Rule 17.2(a)).  * Certified copies not received:  Applicant has THREE MONTHS FROM THE "MAILING DATE"	nder 35 U.S.C. § 119(a)-(d)  been received.  been received in Application cuments have been received	or (f). on No ed in this national stage application fr	
noted below. Failure to timely comply will result in ABANDONN THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.  4. A SUBSTITUTE OATH OR DECLARATION must be subm INFORMAL PATENT APPLICATION (PTO-152) which give	itted. Note the attached EX		E OF
5. $\square$ CORRECTED DRAWINGS ( as "replacement sheets") mus	et be submitted.		
(a) I including changes required by the Notice of Draftspers	•	w ( PTO-948) attached	
1) ☐ hereto or 2) ☐ to Paper No./Mail Date			
<ul> <li>(b) including changes required by the attached Examiner's         Paper No./Mail Date</li> <li>Identifying indicia such as the application number (see 37 CFR 1 each sheet. Replacement sheet(s) should be labeled as such in the state of the sheet.</li> </ul>	.84(c)) should be written on	the drawings in the front (not the back	) of
6. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.			
Attachment(s)  1. ☐ Notice of References Cited (PTO-892)  2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)  3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date  4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	6. ⊠ Interview S Paper No 7. ⊠ Examiner's 8. ⊠ Examiner's	nformal Patent Application Summary (PTO-413), /Mail Date <u>03/10/10</u> . s Amendment/Comment s Statement of Reasons for Allowanc Continuation Sheet.	e

Continuation of Attachment(s) 9. Other: Claim Listing for Examiner's Amendment.

## **DETAILED ACTION**

## **EXAMINER'S AMENDMENT**

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Applicants' Attorney, Mr. Eric J. Robinson on 03/10/2010.

An attachment to this Office Action was requested by the Examiner and provided by the Applicant in accordance with MPEP § 1302.04.

The application has been amended as follows:

In the claims of the "After Final Amendment" filed on 02/16/2010:

Claims 1-69 have been amended as shown on the attached claim listing.

## Allowable Subject Matter

2. Claims 8, 12-14, 22, 26-29, 33-35, 43-46, 48, 51-54, 56, 59-62, 64, and 67-69 are allowed which have been re-numbered to as 1, 2-3, 6-9, 11-14, 5, 10, and 15-30, respectively.

The following is an examiner's statement of reasons for allowance:

Regarding independent **claim 8**, the prior art of record fails to teach or suggest an audio processing circuit comprising a first chip capacitor mounted over a flexible printed circuit connected to the insulating substrate, the first chip capacitor being electrically connected to a second terminal of the second thin film resistor, and

a smoothing circuit and the smoothing circuit comprises a third thin film resistor and a second chip capacitor,

wherein a first terminal of the third thin film resistor is electrically connected to the first thin film resistor, and

wherein a second terminal of the third thin film resistor is connected to the second chip capacitor

in combination with other limitations, as specified in the independent Claim 8.

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Regarding independent **claim 22**, the prior art of record fails to teach or suggest a display device comprising a first chip capacitor mounted around the pixel portion and over the insulating substrate, the first chip capacitor being electrically connected to a second terminal of the second thin film resistor, and

a smoothing circuit and the smoothing circuit comprises a third thin film resistor and a second chip capacitor,

wherein a first terminal of the third thin film resistor is electrically connected to the first thin film resistor, and

wherein a second terminal of the third thin film resistor is connected to the second chip capacitor

in combination with other limitations, as specified in the independent Claim 22.

Regarding independent **claim 29**, the prior art of record fails to teach or suggest a display device comprising a first chip capacitor mounted over a flexible printed circuit connected to the insulating substrate, the first chip capacitor being electrically connected to a second terminal of the second thin film resistor, and

a smoothing circuit and the smoothing circuit comprises a third thin film resistor and a second chip capacitor,

wherein a first terminal of the third thin film resistor is electrically connected to the first thin film resistor, and

wherein a second terminal of the third thin film resistor is connected to the second chip capacitor

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in combination with other limitations, as specified in the independent Claim 29.

Regarding independent **claim 46**, the prior art of record fails to teach or suggest an audio processing circuit comprising a first chip capacitor mounted over the insulating substrate, the first chip capacitor being electrically connected to a second terminal of the second thin film resistor, and

a smoothing circuit and the smoothing circuit comprises a third thin film resistor and a second chip capacitor,

wherein a first terminal of the third thin film resistor is electrically connected to the first thin film resistor, and

wherein a second terminal of the third thin film resistor is connected to the second chip capacitor

in combination with other limitations, as specified in the independent Claim 46.

Regarding independent **claim 54**, the prior art of record fails to teach or suggest an audio processing circuit comprising a first chip capacitor mounted over a printed circuit board electrically connected to the insulating substrate, the first chip capacitor being electrically connected to a second terminal of the second thin film resistor, and

a smoothing circuit and the smoothing circuit comprises a third thin film resistor and a second chip capacitor,

wherein a first terminal of the third thin film resistor is electrically connected to the first thin film resistor, and

wherein a second terminal of the third thin film resistor is connected to the second chip capacitor

in combination with other limitations, as specified in the independent Claim 54.

Regarding independent **claim 62**, the prior art of record fails to teach or suggest a display device comprising a first chip capacitor mounted over a printed circuit board electrically connected to the insulating substrate, the first chip capacitor being electrically connected to a second terminal of the second thin film resistor, and a smoothing circuit and the smoothing circuit comprises a third thin film resistor and a second chip capacitor,

wherein a first terminal of the third thin film resistor is electrically connected to the first thin film resistor, and

wherein a second terminal of the third thin film resistor is connected to the second chip capacitor

in combination with other limitations, as specified in the independent Claim 62.

Claims 12-14 and 43 are allowed by virtue of their dependency on Claim 8.

Claims 26-28 and 44 are allowed by virtue of their dependency on Claim 22.

Claims 33-35 and 45 are allowed by virtue of their dependency on Claim 29.

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Claims 48 and 51-53 are allowed by virtue of their dependency on Claim 46. Claims 56 and 59-61 are allowed by virtue of their dependency on Claim 54.

Claims 64 and 67-69 are allowed by virtue of their dependency on Claim 62.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

## Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CON P. TRAN whose telephone number is (571)272-7532. The examiner can normally be reached on M - F (08:30 AM - 05:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor VIVIAN C. CHIN can be reached on 571-272-7848. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

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you have questions on access to the Private PAIR system, contact the Electronic

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Business Center (EBC) at 866-217-9197 (toll-free).

/CPT/ March 24, 2010

/Vivian Chin/

Supervisory Patent Examiner, Art Unit 2614